IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re appli	cation of:	Art Unit: Not assigned
YAEGASH	II et al.	Examiner: Not assigned
Serial No:	Not assigned (parent 10/429,460)	
Filed:	January 29, 2004	·
For:	NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE AND ITS	

	ISMITTAL OF INFORMATION LOSURE STATEMENT
P.O. B	issioner for Patents ox 1450 ndria, VA 22313-1450
Dear S	Birs:
1. 🛚	The information disclosure statement submitted herewith is being filed within three months of the filing date of the application other than a continued prosecution application, or within three months of the date of entry into the national stage of an international application, or before the mailing date of a first Office Action on the merits, or before the mailing of a first Office action after the filing of a request for continued examination under §1.114, whichever event occurs last. 37 C.F.R. §1.97(b).
2. 🗌	The information disclosure statement transmitted herewith is being filed after the period specified in §1.97(b), but before the mailing date of a final action under §1.113, or a notice of allowance under §1.311, or an action that otherwise closes prosecution in the application, whichever occurs first. A statement specified in §1.97(e) or a fee set forth in §1.17(p) is included. 37 C.F.R. §1.97(c).
	§1.97(e) STATEMENT
	I, the person signing below, state:
	that each item of information contained in the information disclosure statement was first cited in the attached communication from a foreign patent office in a counterpart foreign application and that the communication is dated not more than three months prior to the filing of the statement. 37 C.F.R. §1.97(e)(1).
	OR
	that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification

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after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in §1.56(c) more than three months prior to the filing of the statement. 37 C.F.R. §1.97(e)(2).

OR FEE Attached is a fee set forth in 37 C.F.R. §1.17(p) for submission of an information disclosure statement under §1.97(c). (\$180.00). [OR:] Please charge the fee set forth in 37 C.F.R. §1.17(p) for submission of an information disclosure statement under §1.97(c) (\$180.00) to Deposit Account No. 50-1314. A copy of this petition is enclosed. The information disclosure statement transmitted herewith is being filed after the period specified in §1.97(c), but before, or simultaneously with the payment of the issue fee. A statement specified in §1.97(e) and a fee set forth in §1.17(p) are included. 37 C.F.R. §1.97(d). §1.97(e) STATEMENT I, the person signing below, state: that each item of information contained in the information disclosure statement was first cited in the attached communication from a foreign patent office in a counterpart foreign application and that the communication is dated not more than three months prior to the filing of the statement. 37 C.F.R. §1.97(e)(1). OR that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in §1.56(c) more than three months prior to the filing of the statement. 37 C.F.R. §1.97(e)(2). AND FEE Attached is a fee set forth in 37 C.F.R. §1.17(p) for submission of an information disclosure statement under §1.97(d). (\$180.00).

4. If it should be determined that for any reason either an insufficient fee or an excessive has been paid, please charge any insufficiency or credit any overpayment necessary to ensure consideration of the information disclosure statement for the above-identified application to Deposit Account No. 50-1314. A copy of this petition is enclosed.

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5.	\boxtimes	C.F.R. § 1.98(d), copies of the listed	e enclosed Form PTO-1449. Pursuant to 37 reference(s) are not provided since they were ial No10/138,849, the benefit of the filing date U.S.C. § 120.
		NON-ENGLISH LAI	NGUAGE REFERENCES
			terpart application. The search report Examiner ancy of any non-English language references cited
	☐ The specification incorporates comments on the relevancy of Non-English language references.		
		Set forth below are comments provide relevancy of non-English language in the second s	ed by the applicant's home country counsel on the references:
			Respectfully submitted,
		·	HOGAN & HARTSON L.L.P.
Da	ıte:	January 29, 2004	By: Anthony J. Orley
Bil	ltmo	ore Tower	Registration No. 41,232
		outh Grand Avenue, Suite 1900	Attorney for Applicant(s)
		ngeles, CA 90071	**************************************
		none: (213) 337-6700	·

Facsimile:

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FORM PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Digest of Technical Papers pages, 66 - 67

Docket Number (Optional) Application Number 81790.0311 Not assigned **Applicant**

YAEGASHI et al.

Filing Date January 29, 2004 **Group Art Unit** Not assigned

		U.S. PATE	NT DOCUMENTS	;				
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DA		
	5,989,957	11-1999	Ngo et al.	438	257			
	5,841,174	11-1998	Arai	257	392			
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	5,600,164	02-1997	Ajika et al.	257	321			
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	F	DREIGN PA	TENT DOCUMEN	ITS	5			
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	62-045165	02-1987	Japan				<u> </u>	
	08-23041	01/23/96	Japan					
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	62-76668	9/30/85	Japan		27/10			
	7-297304	3/24/95	Japan		21/8247			
	OTHER DOCUME	NTS (Including	Author, Title, Date, Pe	ertinent Pages	s, Etc.)			
	ANNON, et al., "0.25 µm Merged igest of Technical Papers pages,		SOI Logic Using Patter	ned SOI", 200	0 Symposium o	n VLSI Tech	nology	
S	CHEUERLEIN, et al., "A 10ns Rea witch in each Cell", ISSCC 2000/S	ad and Write Nor Session 7/TD: En	n-Volatile Memory Arra nerging Memory & Devi	y Using a Mag ce Technologi	netic Tunnel Jur es/ Paper TA 7.	nction and F 2, pages12	ET 8 - 129	
	YAMADA, et al., "An Embedded DRAM Technology on SOI/Bulk Hybrid Substrate Formed with SEG Process for High-End SOC Application", 2002 Symposium On VLSI Technology Digest of Technical Papers, pages 112 – 113							
Н.	HANNON, et al., "0.25 µm Merged Bulk DRAM and SOI Logic Using Patterned SOI", 2000 Symposium on VLSI Technology							

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

Wolf, et al. "Silicon Processing for the VLSI Era," 1986, Lattice Press, Vol. 1, pages 384-388